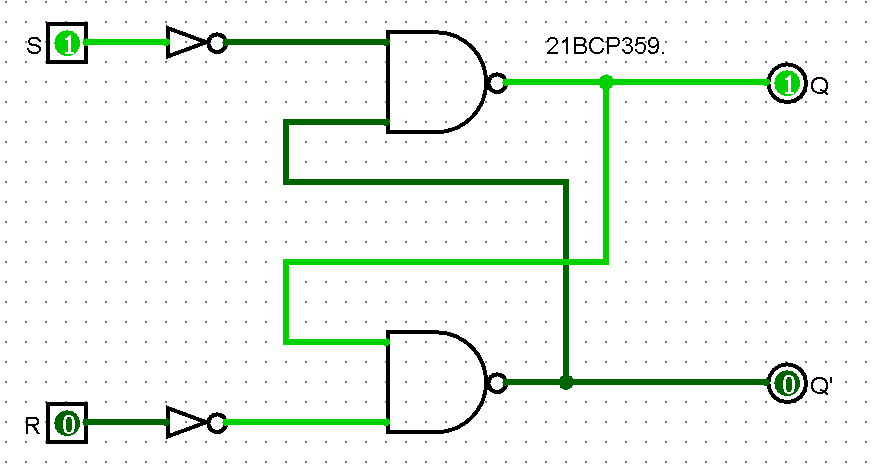
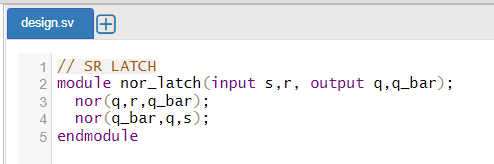
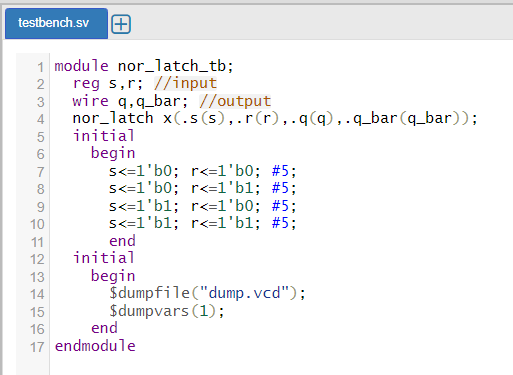
**LAB 8: Sequential Circuits: Latch And SR Flip Flop**

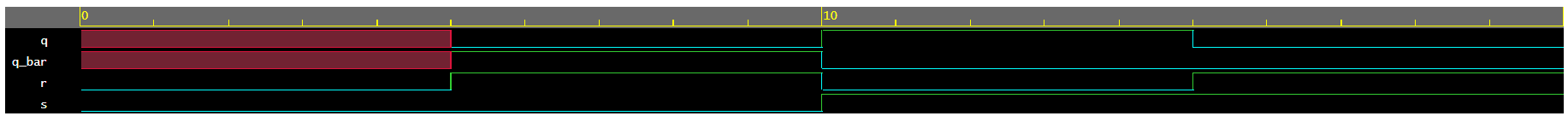
**Question 1: Design an SR flip-flop using Logisim.**

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**Question 2: Write a module for NOR gate and develop a structural Verilog code for the S-R latch using the NOR gate module.** **Validate the code via a suitable Testbench code.**

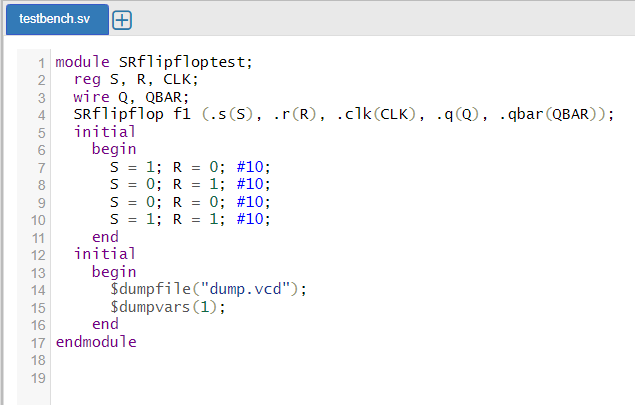
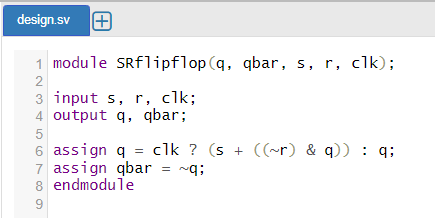
**Expression:** Qn+1 = E.D + E'.Qn

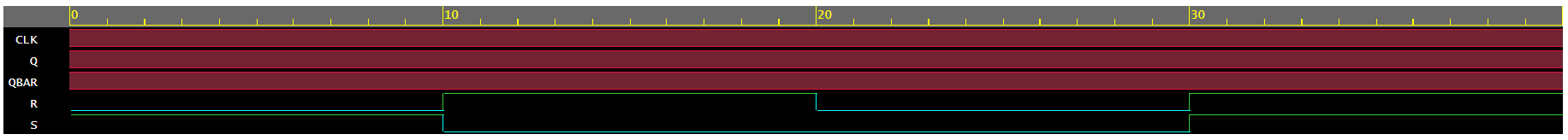
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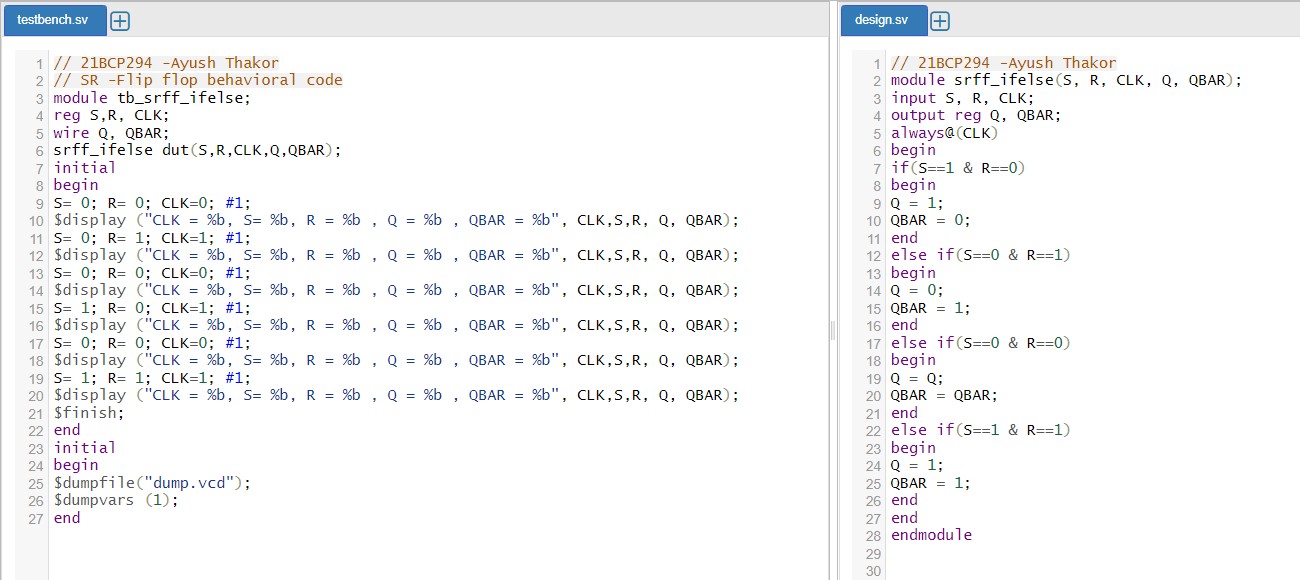
****

**Question 3: Write a Verilog module for NAND gate and utilize it to develop a structural Verilog module. Validate it using suitable Test bench.**

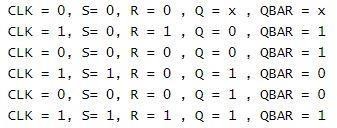
**Expression:** Qn+1 = S + QnR’

****  ****

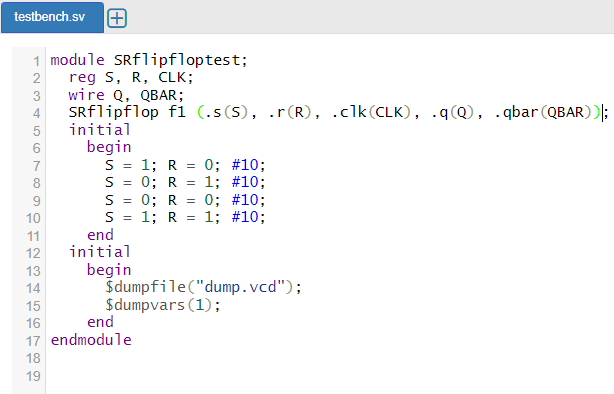
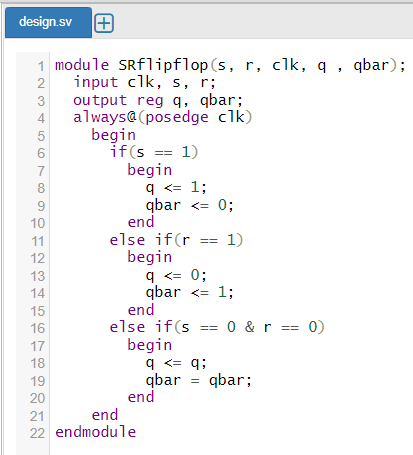
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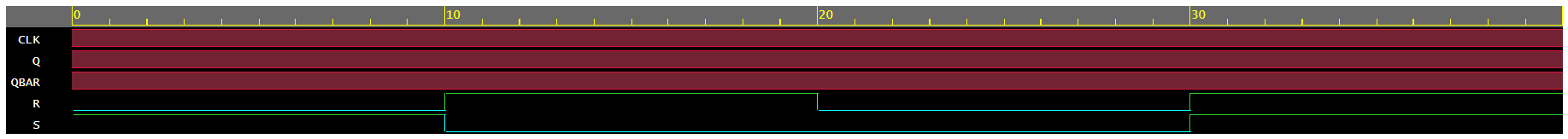
**Q 4. Develop a similar behavioral code and test bench for S-R flip flop using if-else condition as per question 3.**



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**Question 5: Develop a similar behavioural code and test bench for S-R flip flop using if-else condition as per question 3.**

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